Digital Circuits and Systems
NOC, Spring 2015
Quiz 4 Solutions

For questions, refer to the Quiz page. Only the solutions are given below.

Q1: Memory elements are constructed with Multiplexers, NAND Gates, or NOR Gates.
Answer : A,B,C

Q2:The following table is a characteristic table of NAND S-R Latch
(Q is present state and Q* is next state)

S	R	Q*
0	0	Undefined(1,1)
0	1	0
1	0	1
1	1	Q

Answer : B

Q3: Characteristic table of Gated D Latch?
(Q(t) is present state and Q(t+1) is next state)

G	D	Q(t+1)
1	0	0
1	1	1
0	X	Q(t)

Answer : B

Q4:At time t_0, the values of (*in, R3, R2, R1, R0*)=(1,0,0,0,0).
The signal 'in' is 1(ON) for 3 clock cycles and it turns OFF.

Time	in	R3	R2	R1	R0
t_0	1	0	0	0	0
t_1	1	1	0	0	0
t_2	1	1	1	0	0
t_3	1	1	1	1	0
t_4	0	1	1	1	1
t_5	0	0	1	1	1
t_6	0	0	0	1	1
t_7	0	0	0	0	1

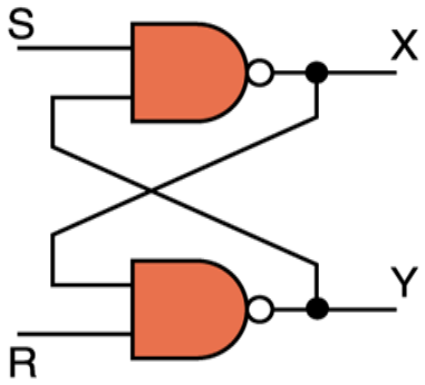
Answer : B

Q5: The following statements are true.

(i) Latches are level triggered and flip-flops are edge triggered.
(ii) Flip-flops are synchronous i.e they have clock signals whereas latches are asynchronous i.e they don't need clock input.

Answer : A , C

Q6: When S=0 and R=0, the following circuit reaches an invalid state



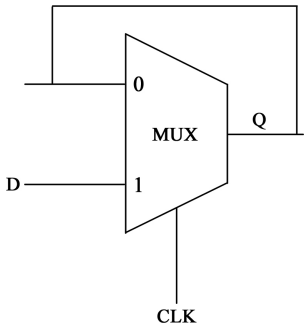
Answer : A

Q7:

Present State			Input			Next State		
q0	q1	q2	D0	D1(q0 xor q2)	D2	q0	q1	q2
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	1	0
1	1	0	0	1	1	0	1	1
0	1	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1	1

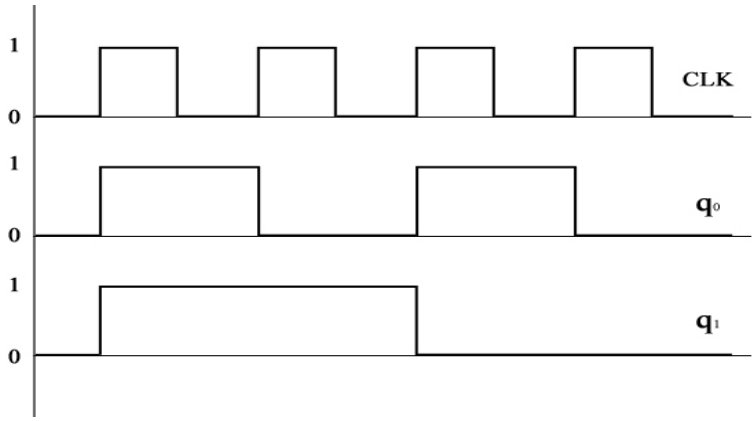
Answer : A

Q8:



Answer : 1

Q9:



Answer : A

Q10:

Clock	Input (Q0 . Q1)	Q3	Q2	Q1	Q0
0		0	1	1	1
1	1	1	0	1	1
2	1	1	1	0	1
3	0	0	1	1	0
4	0	0	0	1	1

Answer : D

Q11:

T	Q'	Q
0	0	0
0	1	1
1	0	1
1	1	0

Minterms (1,2) evaluates to TQ' + T'Q

Answer : A